Birzeit University

Department of Electrical and Computer Engineering

ENCS 437 – Computer Architecture

Second Semester 2014/2015 – Midterm Exam

26/3/2015, 3:00 pm

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Instructions:

1) This exam is open-book, open-notes, open-computer, closed-cellphone, and closed-Wi-Fi.
2) Exam duration is 75 minutes.
3) Answer the questions on this exam paper.

Student name: _____ Student Number: _____.

Question	Full Mark	Your Mark	ABET outcome		
			a	c	e
1	6		*		
2	6			*	
3	4			*	
4	8			*	
5	6			*	*
Total	30				

Question 1: (6 marks)

Suppose that you have been running a program on your PC that has 300MHz Pentium II processor. By running a detailed simulator, you were able to collect the following instruction mix and the CPI for each instruction type:

Instruction Class	Frequency (%)	Cycles
Integer arithmetic and logical	40	1
Load	20	1
Store	10	2
Branches	20	3
Floating Point	10	5

A. What are the CPI and the MIPS ratings of the Pentium II for this program?

CPI = 0.4 * 1 + 0.2 * 1 + 0.1 * 2 + 0.2 * 3 + 0.1 * 5 = 1.9 cycles per instruction **(1 mark)**

MIPS = (clock rate / CPI) * 10^{-6} = (300 * 10^{6} / 1.9) * 10^{-6} ~= 158 MIPS **(1 mark)**

B. Now, suppose that the Pentium III has just been introduced with a faster clock rate (450 MHz). However, in order to make the clock rate faster, the Pentium engineers had to increase the CPI for arithmetic, logical, and load instructions to 2 cycles and floating point instructions to 6 cycles. What is the speedup of the Pentium III over the Pentium II on the same program above?

CPI_{new} = 0.4 * 2 + 0.2 * 2 + 0.1 * 2 + 0.2 * 3 + 0.1 * 6 = 2.6 cycles per instruction **(1 mark)**

Speedup = Execution $time_{old}$ / Execution $time_{new}$

= (I * CPI_{old} /clock $rate_{old}$) / (I * CPI_{new} /clock $rate_{new}$)

= $(1.9 / 300 * 10^6) / (2.6 / 450 * 10^6)$

~= 1.1 **(1 mark)**

C. The engineers for Pentium Company are currently working on the Pentium IV. Instead of increasing the clock rate again, they are working on reducing the time for the floating-point instructions (after the enhancement made in part B). Use Amdahl's law to show the maximum speedup that you could expect between the Pentium III and Pentium IV on the same program. Assume the clock rate for both processors is 450 MHz?

F = portion of program affected by enhancement

= 0.1 * 6 / (0.4 * 2 + 0.2 * 2 + 0.1 * 2 + 0.2 * 3 + 0.1 * 6) = 0.6/2.6 ~= 0.23 **(1 mark)**

Speedup = 1 / ((1-F) + (F/S))

Maximum speedup is when S is ∞

$Speedup_{max}$ = 1 / (1-F) = 1 / (1-0.23) ~=1.3 **(1 mark)**

Question 2: (6 marks)

Show the Y86 assembly instructions equivalent to the following machine code:

0x202340030001000061327402010000

Assume that the code is stored at the address 0x100

Address	Machine code	Y86 Assembly code
0x100	0x2023	rrmovl %edx, %ebx
0x102	0x400300010000	rmmovl %eax, 0x100(%ebx)
0x108	0x6132	subl %ebx, %edx
0x10A	0x7402010000	jne (0x102)

(1.5 marks for each instruction)

Question 3: (4 marks)

In the program you obtained in question 2:

a) Identify data hazards.

1- A data hazard on %ebx between the first and second instruction. **(1 mark)**

2- A data hazard on %ebx between the first and third instruction. **(1 mark)**

(A non-hazard identified as a hazard will lose you 1 mark)

b) Describe a scenario in which there will be branch misprediction.

A branch misprediction will occur if the jump condition is false. This will happen if the result of subtraction in the third instruction is zero, i.e. if %ebx and %edx have the same value. This will *always* be the case since the first instruction copies %ebx into %edx. **(2 marks)**

Question 4: (8 marks)

Assume that the code in question 2 above is executed by the PIPE- design (Textbook, Figure 4.41, page 403). Show the values of the signals **D_valC, D_valP, E_valA, E_valB, and M_valE** in the clock cycles listed below.

If the value is unknown but the source is known, write the source.

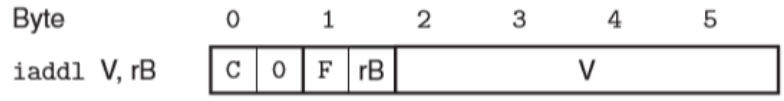
If the value and the source are both unknown, write "N/A".

Cycle	D_valC	D_valP	E_valA	E_valB	M_valE
1	N/A	N/A	N/A	N/A	N/A
2	N/A	0x102	N/A	N/A	N/A
3	0x100	0x108	R[%edx]	0	N/A
4	N/A (or same)	0x10A	R[%eax]	R[%ebx]	0 + R[%edx]
5	0x102	0x10F	R[%ebx]	R[%edx]	0x100+R[%ebx]
6	0x100	0x108	N/A (or same)	N/A (or same)	R[%edx]-R[%ebx]
7	N/A (or same)	0x10A	R[%eax]	R[%ebx]	N/A (or same)

(Each mistake will lose you 1/2 mark)

Question 5: (6 marks)

Suppose we want to add the new instruction iaddl with the following format:



This instruction adds the constant V to register rB.

a) Modify the signal aluA (page 388) to accommodate this change.

For this new instruction, aluA = valC, thus the modified equation is: **(2 marks)**

```
int aluA = [ icode in { IRRMOVL, IOPL } : valA;
             icode in { IIRMOVL, IRMMOVL, IMRMOVL, IIADDL } : valC;
             icode in { ICALL, IPUSHL } : -4;
             icode in { IRET, IPOPL } : 4; # Other instructions don't need ALU
             ];
```

b) Modify the signal aluB (page 465) to accommodate this change.

For this new instruction, aluB = valB, thus the modified equation is: **(2 marks)**

```
int aluB = [
             icode in { IRMMOVL, IMRMOVL, IOPL, ICALL, IPUSHL, IRET, IPOPL, IIADDL } : valB;
             icode in { IRRMOVL, IIRMOVL } : 0; # Other instructions don't need ALU
             ];
```

c) What additional signal(s) ought to be modified?

The signals srcB, dstE, set_cc, need_regid, need_valC, and instr_valid ought to be modified to include this new instruction.

(2 marks, for 2 signals)